## MP 5.2 Fully-Integrated SONET OC48 Transceiver in Standard CMOS

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This fully-integrated, SONET OC-48 (2.488/2.666 Gb/s) transceiver uses a standard CMOS process. Design techniques, and use of standard CMOS technology allows performance exceeding the SONET requirements while achieving reduced power dissipation, higher integration levels, and simplified manufacturability as compared to other fabrication technologies. This chip, designed using standard 0.18µCMOS has 500mW total power dissipation and 1ps rms jitter.

This device contains clock and data recovery (CDR) and 1:4 demux in its receive path and a clock multiplication unit (CMU) along with 4:1 mux in its transmit path (Figure 5.2.1). The operating frequency is selectable at either 2.488Gb/s or, if forward error correction (FEC) is implemented, 2.666Gb/s. The CDR generates a clock that is at the same frequency as the incoming serial data bit rate. This clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern. The demux then converts this retimed data to four 622 (666)Mb/s LVDS parallel channels. On the transmit side, a 4b 622 (666)Mb/s LVDS input data is clocked into a digital FIFO which compensates for phase variations between the on-chip clock and the input clock that accompanies the LVDS input data. This on-chip timing domain is established in the CMU, where a high frequency, low jitter phase-locked loop generates the 2.488 (2.666)GHz transmit clock by multiplying the 77.76 (83.31) or 155.52 (166.63)MHz reference clock by 32 or 16, respectively. The FIFO output data is then converted to a 2.488 (2.666)Gb/s serial stream and driven off chip. The high-speed data and clock output drivers consist of a differential pair designed to drive a 50Ω transmission line.

The CDR consists of two loops (Figure 5.2.2); the first one acquires frequency lock to the reference clock and the second one phase locks to the incoming data. A digital lock detect circuit monitors the frequency difference between the divided version of the extracted clock and the reference clock; as soon as they are within 400ppm, the phase acquisition loop is enabled. The frequency pulling range of this loop exceeds 450ppm to ensure that frequency lock performance is robust. To increase the noise immunity of the CDR, the entire loop, including the charge pump and the loop filter, uses fully differential design. Figure 5.2.3 shows this differential charge pump where a unity-gain buffer-based architecture is used due to its speed advantage [1], and a common-mode feedback circuit is added to keep the voltage-controlled oscillator (VCO) control voltage at the optimum value. This common-mode feedback circuit also rejects any common-mode noise due to the power supply or substrate. Furthermore, an LC VCO has been chosen due to its low phase noise performance. To optimize its phase noise special attention is paid to maximize the Q of its on-chip spiral inductor and varactors. Moreover, the sizes of VCO transistors are selected so that the output waveform is symmetrical to minimize the phase noise $1/f^3$ region [2]. The CMU phase lock loop (PLL) is similar to the CDR frequency acquisition loop where a differential charge pump and loop filter feed a LC-based VCO.

One of the key parameters in PLL design is loop bandwidth. This bandwidth directly affects the three main SONET jitter specs; jitter generation, transfer, and tolerance. For jitter generation, there is a trade-off between the suppression of input jitter and the intrinsic VCO jitter. This is due to the fact that a PLL exhibits a low-pass jitter transfer characteristic between its input and output, but exhibits a high-pass characteristic between the VCO input and PLL output. Moreover, SONET jitter transfer requirements place an upper limit on this bandwidth, while jitter tolerance sets a lower one. A bandwidth of 1.8MHz is the optimum value for our design. This loop filter consists of a series resistor R and a capacitor C1 in parallel with another capacitor C2. The jitter bandwidth is given by Icp·Kvco·R, where Icp is the charge pump current and Kvco is the VCO gain. The value of this resistor is obtained based on a bandwidth of 1.8MHz. Moreover, C1 and C2 values have been chosen to not only minimize the peaking in the jitter transfer curve and the amount of output jitter, but also to maximize the frequency pulling range of CDR phase acquisition loop. Figure 5.2.4 shows the frequency spectrum of the CMU output clock with these optimized values.

The low power dissipation of the chip is achieved in a number of ways. First, sub-micron CMOS processes use low power supply voltages (1.8V for this chip), which automatically results in lower power consumption. Also, the low speed section of the chip uses traditional rail-to-rail logic where there is no static current, further reducing the dissipation. The entire FIFO and all the digital blocks consume <20mW. Finally, integration of CDR, demux, CMU, and mux on one chip leads to elimination of power-hungry chip-to-chip interfaces, thereby reducing power dissipation to less than one-fourth of existing solutions in other technologies (SiGe, GaAs, BICMOS) [4,5]. As the power consumption is reduced, less heat is generated and a smaller package can be used. This chip is in a 14x14x1.4mm$^3$, 100-pin LQFP package.

To minimize cross talk, all blocks that are running at different frequencies are isolated from each other using rings of substrate ties. These rings are especially effective in CMOS processes with bulk substrate.

Through the use of the techniques described above, the jitter performance objective is met. The typical jitter generation measurement of the transmitted clock is approx. 2.5mUI rms (1ps rms), which is one-fifth of a previously published 2.5GHz CMOS transceiver [3]. Note that this jitter performance meets or exceeds circuits built in other, more expensive, technologies while exhibiting far lower power dissipation [4]. Measurement results show power consumption of the entire transceiver including all IOs to be 500mW from a 1.8V power supply. Furthermore, this chip exceeds all other SONET jitter requirements. Figure 5.2.5 shows the measured eye diagram of the transmitted serial data. Figure 5.2.6 summarizes the measured performance. Figure 5.2.7 is a chip micrograph.

*References:*

[1] M. Johnson and E. Hudson, "A variable delay line PLL for CPU-coprocessor synchronization," IEEE J. Solid-State Circuits, vol. 23, pp. 1218-1223, Oct. 1988.
[2] A. Hajimiri and T. Lee, "A general theory of phase noise in electrical oscillators," IEEE J. Solid-State Circuits, vol. 33, pp. 179-194, Feb. 1998.
[3] R. Gu, et al "A 0.5-3.5Gb/s Low power low jitter serial data CMOS transceiver," ISSCC Digest of Technical Papers, pp. 352-353, Feb. 1999.
[4] "OC48 SONET/SDH/ATM 4-Bit Transceiver Specifications," Applied Micro Circuits Corporation, S3457.
[5] "Multi-Rate SONET/SDH Clock Recovery Unit Specifications," Applied Micro Circuits Corp., S3056.

 

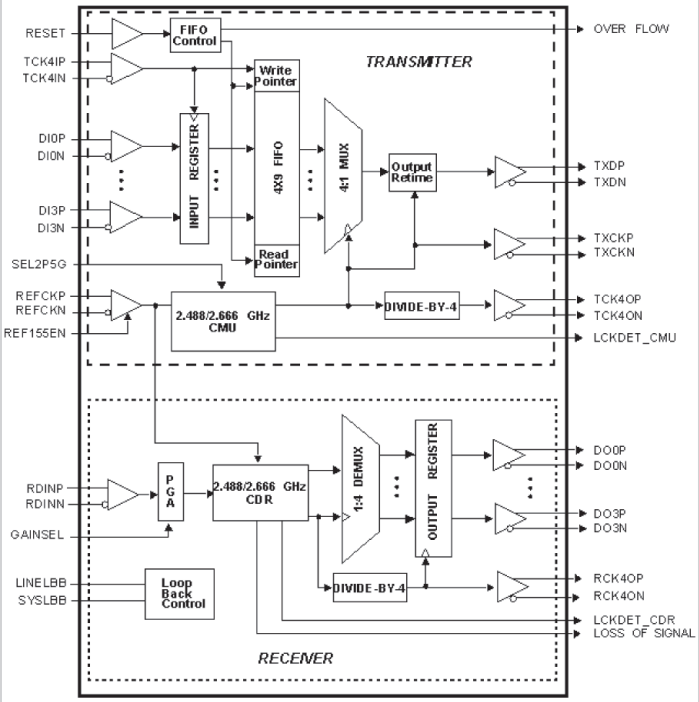


Figure 5.2.1: Chip top-level block diagram.

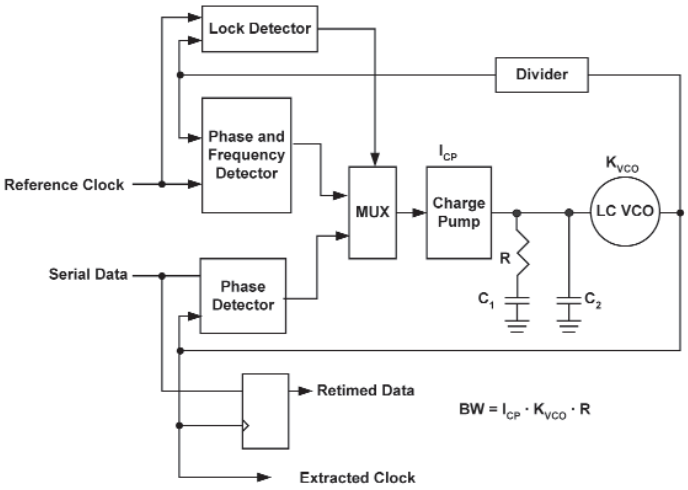


Figure 5.2.2: Clock and data recovery block.

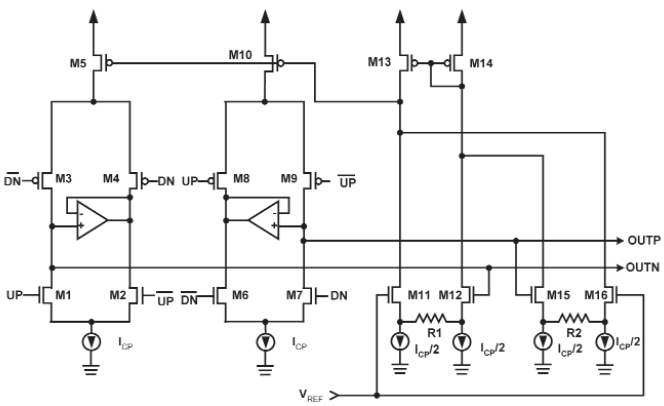


Figure 5.2.3: Differential charge pump.

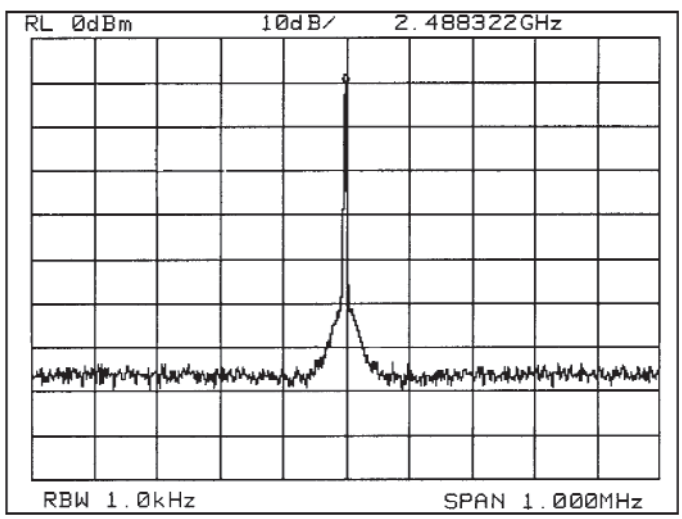


Figure 5.2.4: Transmitted clock frequency spectrum.

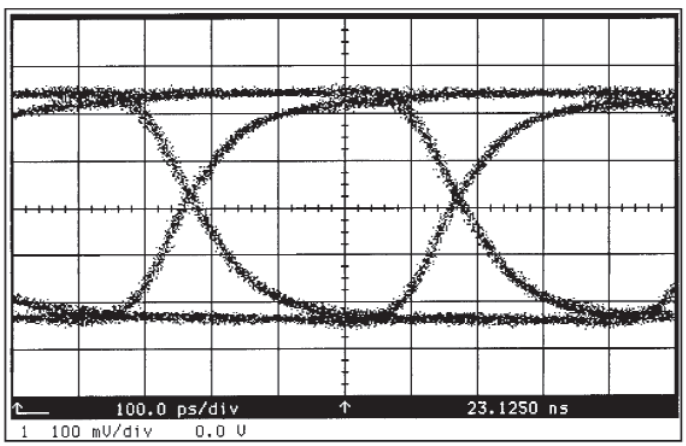


Figure 5.2.5: Eye diagram of serial transmitted data at 2.488Gb/s.

| | |
|---|---|
| Transmitted clock rms jitter | 1 ps |
| Transmitted serial data eye width | 360 ps |
| Transmitted serial data swing | 470 mV |
| Receiver jitter transfer bandwidth | 1.8 MHz |
| Receiver jitter tolerance | Exceeds OC-48 Telcordia mask |
| Supply voltage | 1.8V |
| Power dissipation | 500 mW |
| Technology | 0.18µ standard CMOS |
| Chip size | 3.2 x 3.8 mm |
| Package | 100-pin LQFP |

**Figure 5.2.6: Summary of measured performance.**

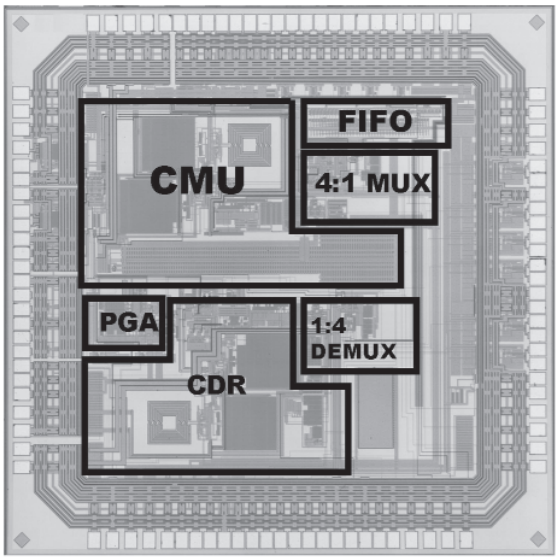


**Figure 5.2.7: Die micrograph of integrated SONET OC48 transceiver.**